Unit III

State Machines

Basic Design steps :-

- What is mean by state Machines ?

– A state machine is a mathematical model of computation that defines a system by a finite number of states, transitions between those states, and actions, which can be based on inputs or outputs.

- Purpose :-

– State machines are widely used in digital electronics for designing of sequential logic circuits, where the system's behavior depends not just on the current inputs but also on the history of the previous ~~output~~ inputs.

- State Machine Components :-

- States :- Distinct condition or configurations of the system, represented typically by binary codes.
- Transitions :- Movement from one state to another, triggered by input signal or clock pulses.
- Input :- Signals or events that cause the state machine to transition from one state to another.
- output :- Actions or signals generated by state machi which can depend on the current state (Moore) or both the state & inputs (Mealy).

- **Clock** :- In synchronous state machines, transitions are controlled by a clock signal.

Basic Design steps :-

* State Table :-

- Truth table is used for explaining the relation bet^n it's inputs and outputs of a combinational circuit. But the use of truth table is not suitable for explaining the i/p o/p relation for a sequential circuit. Instead we use the state table for the sequential circuits.
- The state table tells us about the relation between the present state, next state & output.
- state table is a systematic approach which is used to analyze the large sequential circuit.

* State Diagram :-

- The information available in the state table is represented graphically using the state diagram.
- The state diagram is drawn by using the state table as a reference. It is used to analyze the behavior of sequential circuit rapidly.
- In state diagram, a state is represented by inside the circle and the transition lines are drawn bet^n the states using directed lines.
- A directed line connecting the same circle indicates that the next state is same as the present state.

- Moore Circuit :-

- In the moore circuit, the o/p is represented inside the circle under the state value and the i/p is represented on the transition line.

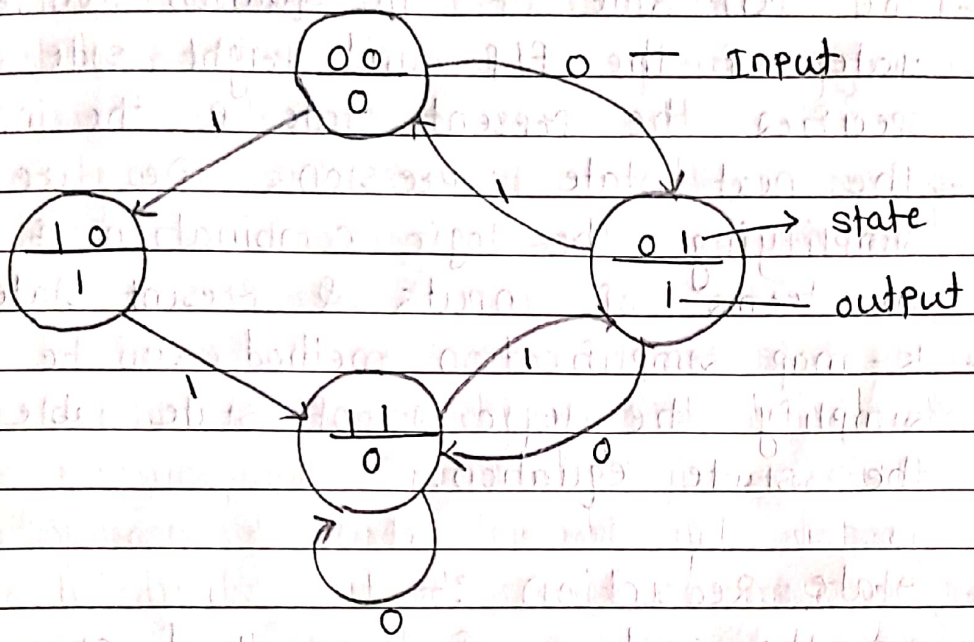


fig:- State diagram of Moore Circuit.

- Mealy Circuit :-

- In the mealy circuit, the o/p is represented on the transition line under the value of i/p & the state is represented inside the circle. The state diagram is obtained from state table of Mealy Circuit.

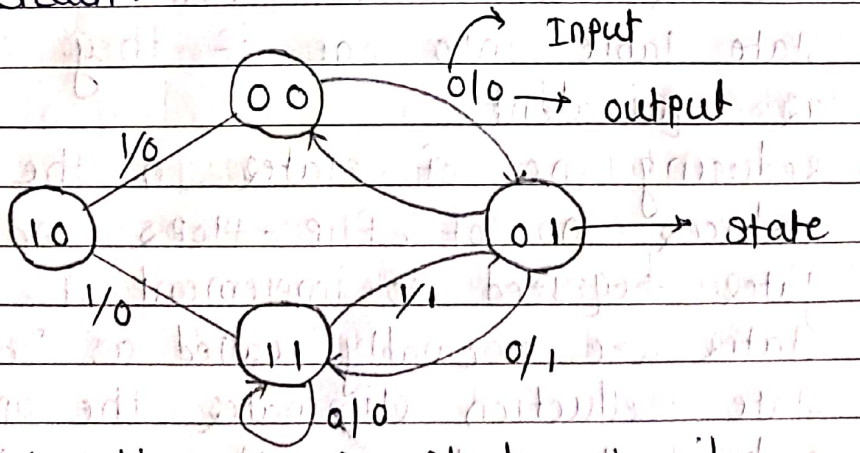


Fig :- State diagram of Mealy circuit.

* State Equation :-

- An algebric expression that specifies the transition of input signal to the output is called state equation or application equation.
- The left side of the equation denotes the next state of the flf and right side of ~~fff~~ eq" specifies the present state & the input.
- The next state expressions ~~we~~ are obtained by simplifying the logic combination of state table in terms of inputs & present state.
- k-map simplification method can be used to simplify the logic s of state table and to obtain the state equation.

* State Reduction :-

- In the analysis of sequential circuit sometimes two different present states exhibit same next states due to the behavioural change of input values.
- These similar types of states can be combined as a single states to reduce no. of states.
- The state reduction procedure for completely specified state table is defined based on the algorithm that is used to combined two states in a state table into one if they provide next state as equivalent.
- Reducing no. of states in the sequential circuit reduces no. of flip-flops and combination of gates required to implement it. The equivalent states are normally called as "redundant state". State reduction eliminates the appearance of redundant state in the state table.

* State Assignment :-

- The process of assigning binary number repren for the physical representation is called as "State Assignment".
- It is necessary to assign the binary number to represent the states in the design of sequential logic circuit.
- For any circuit with M no. of states requires N number of binary bits to assign the binary no. to the states where $2^N \geq M$.
- For example, if we have five states then the state assignment needed by 3 bits to assign state in binary form.
- The remaining states present with binary repren are called as "unused states" which are normally considered as "don't care" conditions during the design.

* Moore and Mealy Machine representation :-

o Moore Circuit :-

- In Moore model, the o/p of synchronous sequential circuit is generate is dependent only on the present state of clock controlled memory element (Flip-flops).
- The functional block diagram of Moore model synchronous sequential circuit is shown below.

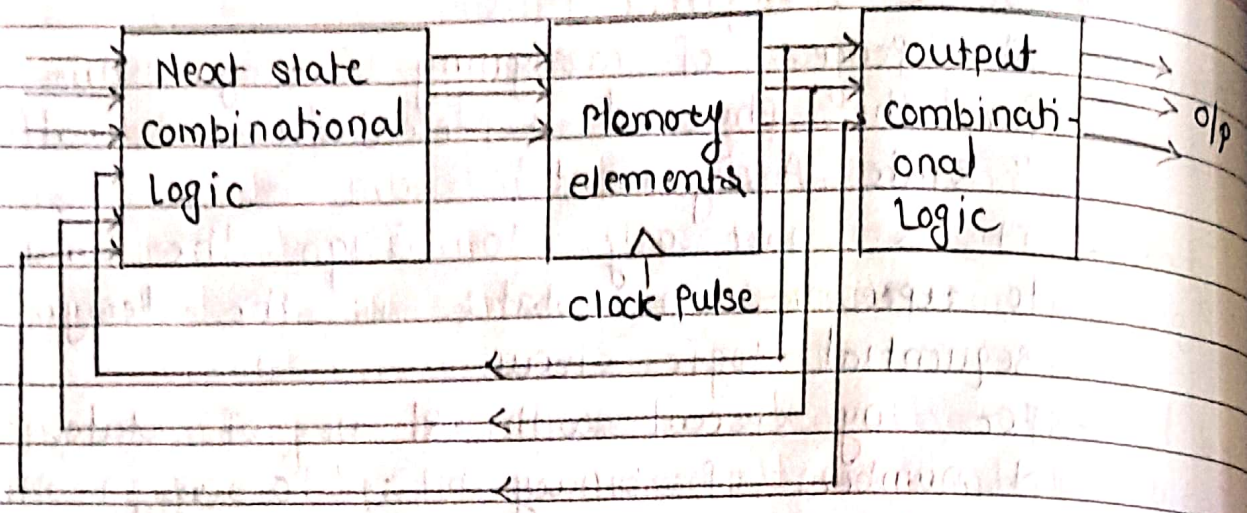


Fig :- Block diagram of Moore Model synchronous sequential circuit.

- It consists of a next state combinational logic circuit, clock controlled memory element & output combinational circuit.
- The next state combinational logic circuit generates the o/p from the inputs and state inputs and the results are stored in the clock controlled memory elements.
- The output logic circuit develops the o/p of sequential circuit from the o/p of memory elements.
- The present state output values of memory element only decides the o/p of sequential circuit through the o/p combinational logic circuit.
- Thus the moore machine provides the o/p always after the active edge of clock pulse.

Mealy Circuit :-

- In Mealy model the o/p of synchronous sequential circuit is generated dependent on the circuit inputs and present state of clock controlled memory elements (Flip-flops).

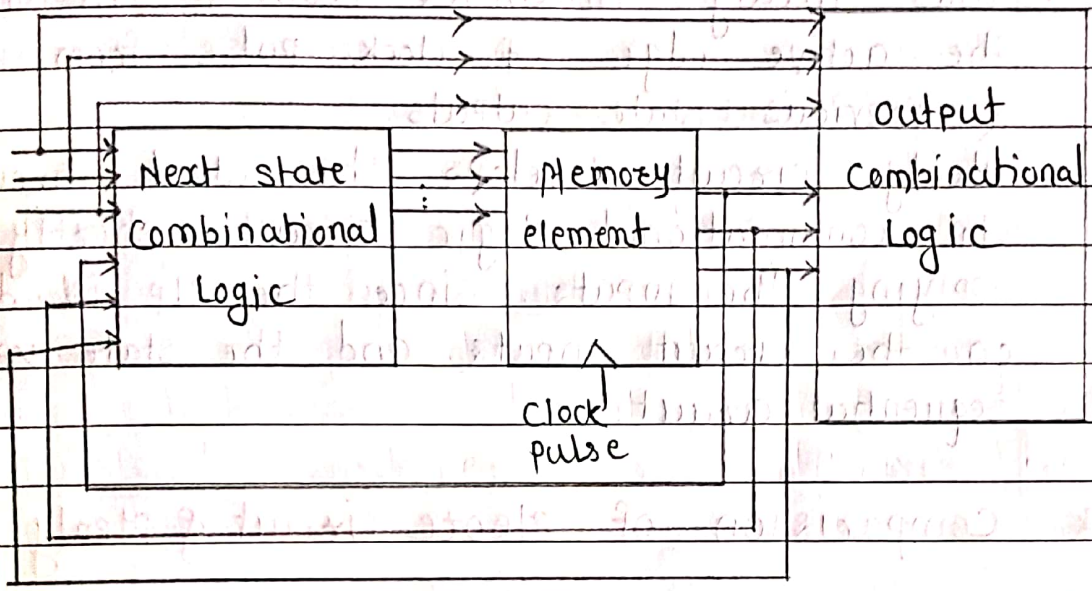


Fig:- Block diagram of Mealy model synchronous sequential circuit.

- The functional block diagram of Mealy model synchronous sequential circuit is shown in fig.
- It consists of a next state combinational logic circuit, clock controlled memory element & o/p combinational circuit.
- The next state combinational logic circuit generates the o/p from the inputs & state inputs and the results are stored in the clock controlled memory elements.

- The output logic circuit develops the o/p of sequential circuit from the o/p of memory elements and circuit inputs.
- The present state output values of memory element and circuit inputs decides the o/p of sequential circuit through the o/p combinational logic circuit.
- Thus mealy machines provides the o/p before the active edge of clock pulse from it inputs & previous state outputs.
- Mealy circuit develops the output through the o/p combinational logic circuit shortly after applying the inputs. Since the o/p is dependent on the circuit inputs and the state i/p of sequential circuit.

* Comparision of Moore circuit & Mealy circuit :-

Sr. No	Moore Circuit	Mealy Circuit
1	Moore circuit is a type of synchronous sequential circuit model which produce the o/p as a fun^n of present state only.	Mealy circuit is a type of synchronous sequential circuit model which produce the o/p as a fun^n of i/p & present state.
2.	The change of i/p do not affect the o/p.	The change of i/p may affect the o/p.

	Moore machine	Mealy machine
3.	Moore machine provides the o/p only after the active edge of clock pulse.	Mealy machine provides the o/p before the active edge of clock pulse from the i/p.
4.	It requires more no. of states to implement the fun^n.	4. It requires less no. of states to implement same fun^n.
5	Example :-  Where Z – output Q_A, Q_0 → state inputs	Example  Where Z – output X – input Q_A, Q_B → state inputs.

* **Implementation :-**

Recommended steps :-

1) It is necessary to first obtain the state table from the given circuit information such as a state diagram, a timing diagram or other pertinent information.

2) The number of states may be reduced by state reduction technique if the sequential circuit can be categorized by i/p o/p relati^n independent of the no. of states.

3) Assign binary values to each state in state table.

4) Determine the no. of F/F needed and assign a letter symbol to each.

5) Choose the types of flip-flop to be used.

6) From the state table, derive the circuit excitn and output tables.

7) Using the k-map or any other simplification method, derive the circuit o/p functions and the F/F input functions.

8) Draw the logic diagram.

* Finite State Machine Implementation :-

- The word finite signifies a finite or limited no. of possible states in the terms of finite state machine.

Advantages of FSM :-

- simple to understand.
- predictable for a given set of inputs and a known as current state, the state transition can be predicted, allowing for easy testing.
- Due to their simplicity, FSM's are quick to design, quick to implement & quick in execution.

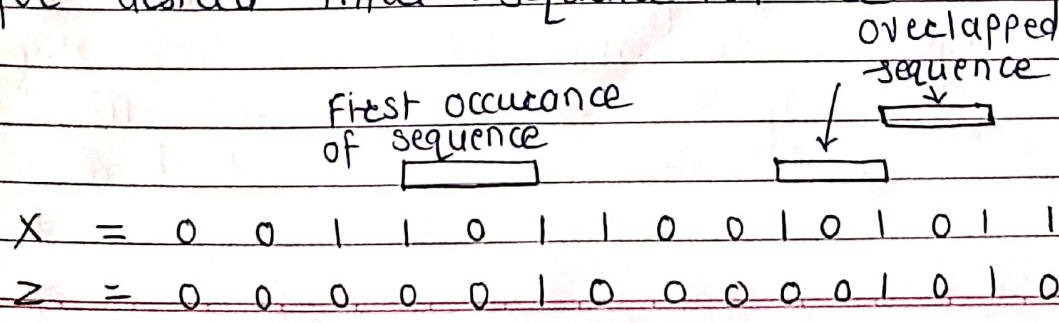
- FSM's are relatively flexible.
- Easy to transfer from a meaningful abstract representation to a coded implementation.

Disadvantages of FSM :-

- The predictable nature of deterministic FSMs can be unwanted in some domains such as computer games.
- Larger systems implemented using a FSM can be difficult to manage and maintain.
- Not suited to all problem domains should only be used when a systems behavior can be decomposed into seperate states, transition & conditions need to be known up front & be well defined.
- The conditions for state transitions are edged, meaning they are fixed.

* Sequence detector :-

- The specified input sequence can be detected using a sequential machine called "Sequence Detector".
- In this circuit output goes high when a prescribed input sequence occurs. A typical i/p sequence & the corresponding output sequence for desired input sequence 101 are.



- As shown above the detection of required i/p sequence can occur in a longer data string & the desired i/p sequence can overlap with another i/p sequence

- It is assumed that i/p can change only bet^n clock pulses. once we know the sequence which is to be detected, we can draw the state dia. ~~we can~~ for it. Then from the state diagram we can design the circuit.

- It is possible to implement sequence detector using both types of sequential machines: Moore machine and Mealy machine.