Unit IV

Digital Logic Families

Classification of Logic Families :-

A digital logic family is a group of compatible devices with the same logic levels and supply voltages. According to components used in the logic family, digital logic family as classified as given below.

Classification of Logic families

- Bipolar
  - Saturated
    - → RTL (Resistor Transistor logic)
    - → DTL (Diode Transistor logic)
    - → DCTL (Direct coupled Transistor logic)
    - → I^2L (Integrated Injection Logic)
    - → HTL (High Threshold Logic)
    - → TTL (Transistor Transistor Logic)
  - Unsaturated
    - → Schottky TTL
    - → ECL (Emitter Coupled logic)
- Unipolar
  - PMOS
    - → (P channel MOSFET)
  - → NMOS (N channel MOSFET)
  - CMOS
    - → (Complementary MOSFET)

Characteristics of Digital IC's :-

1 Speed of operation :-

* Propagation Delay

Propagation delay of a gate is basically the time interval bet^n the application of an I/P pulse and the occurance of the resulting output pulse. The propagation delay is a very important characteristics of logic circuits because it limits the speed at which they can operate.

- The shorter the propagation delay the higher speed of the circuit and vice versa.

- The propagation delay is determined using two basic time intervals.

1. t_{PLH} : It is the time delay measured when o/p is changing from logic 0 to logic 1 state (low to high).

2. t_{PHL} : It is the delay time measured when o/p is changing from logic 1 to logic 0 state (High to Low).

2 Power dissipation :-

The amount of power that an IC dissipate is determined by the average supply current I_{CC} that it draws from the V_{CC} supply. It is the product of I_{CC} and V_{CC} for IC's the value of I_{CC} for Low gate output (I_{CCL}) is different from a High o/p (I_{CCH}).

Therefore average Icc is determined based on the 50 % duty cycle operation of the gate.

$$I_{CC(avg.)} = \frac{I_{CCH} + I_{CCL}}{2}$$

This can be used to calculate avg. power dissipation

$$P_{D(avg.)} = I_{CC(avg.)} \times V_{CC}$$

3. Figure of Merit (Speed Power Product) :-

In general for any digital IC it is desirable to have shorter propagation delays. (higher speed) and lower values of power dissipation. There is usually a trade off bet^n switching - speed & power dissipation in the design of a logic circuit i.e speed is gained at the expense of increased power dissipation. Therefore a common means for measuring & comparing the overall performance of an IC family is the speed power product (SPP). It is also called as "Figure of Merit".

4. Fan In :-

The fan in of a digital logic gate refers to the no. of inputs.

e.g. An inverter has a fan in of 1, 2 i/p NOR gate has a fan in of 2 etc.

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5. Fan out :-

The max^m no. of inputs of the same IC family that the gate can drive maintaining its output level within the specified limits.
e.g. A logic gate of fan out 10 can drive max^m 10 logic inputs from the same family.

o Current & voltage parameters :-

V_{IH} (min) High level input vtg :-

It is the min^m vtg level required for a logical 1 at an input. Any vtg below this level will not be accepted as a HIGH by the logic circuit

V_{IL} (max) Low level input vtg :-

It is the max^m voltage level required for a logic 0 at an i/p. Any vtg above this level will not be accepted as a low by the logic circuit.

V_{OH} (min) High level output vtg :-

It is the min^m voltage level at a logic ckt. o/p in the logical 1 state under defined load condition.

V_{OL} (max) Low level output vtg :-

It is the max^m voltage level at a logic ckt o/p in the logical 0 state under defined load condition.

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I_{IH} High Level i/p current :-

It is the current that flows into an i/p when a specified high level vtg is applied to that i/p.

I_{IL} Low level i/p current :-

It is the current that flows into an i/p when a specified low level vtg is applied to that i/p.

I_{OH} High level o/p current :-

It is the current that flows from an o/p in the logical 1 state under specified load conditions.

I_{OL} Low level o/p current :-

It is the current that flows from an o/p in the logical 0 state under specified load conditions.

- **Noise immunity :-**

Noise immunity is defined as the ability of a logic circuit to tolerate the noise without causing any unwanted changes in the o/p.

A quantitative measure of noise immunity is called as "Noise Margin".

o Operating temperature :-

The temperature range acceptable for the consumer & industrial applications is 0° to 70°c and for the military applications is -55°c to 125

- The performance of gates will be in the specific limits over these temperature ranges.

o Power supply requirements :-

Most of the digital IC's operate on +5V dc supply for it's operation.

o TTL Logic (Transistor transistor Logic) :-

TTL is named for its dependence for on transistor's alone to perform basic logic operation.

* Operation of TTL NAND gate :-

Fig. shows the circuit diagram of 2 i/p multiple NAND gate. Its i/p structure consist of emitter transistor and o/p structure consists of totempole o/p. Here Q_1 is an NPN transistor having two emitters, one for each i/p to gate.

- Although this circuit looks complex, we can simplify its analysis by using the diode equivalent of the multiple emitter transistor Q_1 as shown in fig. b) Diode D_2 & D_3 represent the two E-B jun^n of Q_1 & D_4 is the collector base (C-B) jun^n.

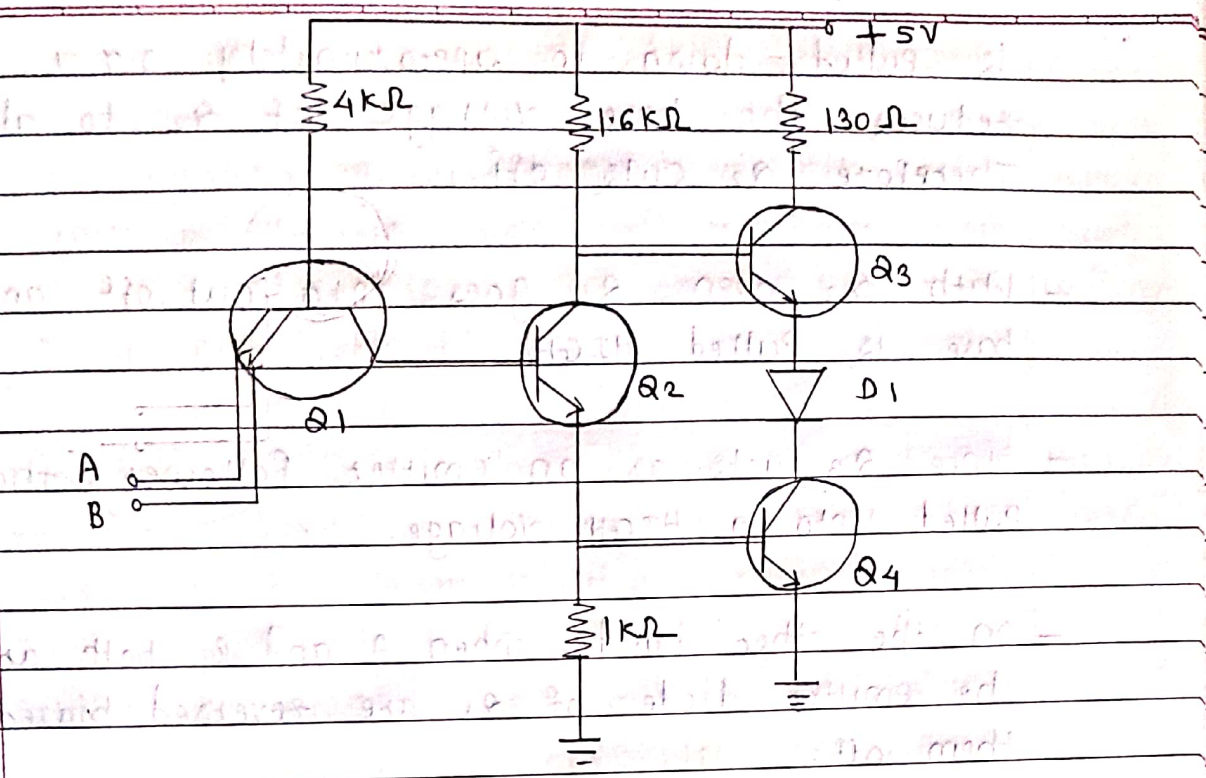

Fig. Two input TTL NAND gate.

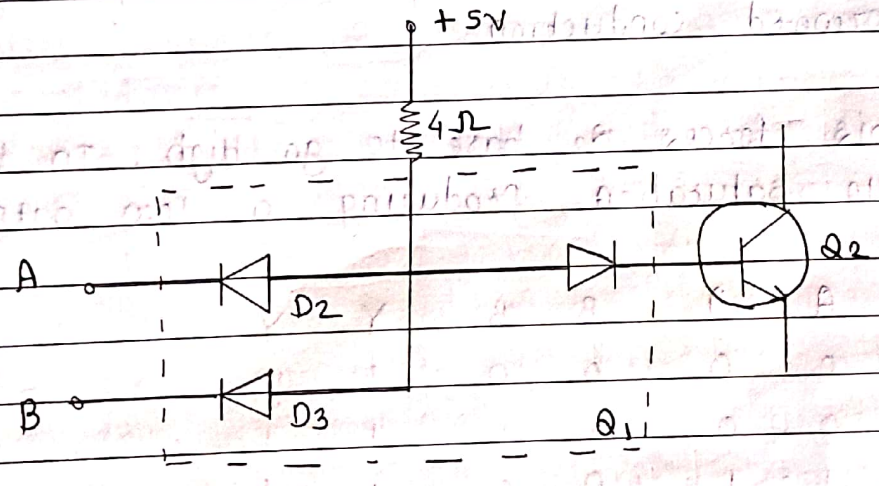

Fig:- Diode equivalent for Q_1

- The i/p vtgs A and B are either Low (ideally grounded) or High (ideally +5V).
- If either A or B or both are low, the corresponding diode conducts and the base of Q_1

is pulled down to approximately 0.7 V. This reduces the base voltage of Q_2 to almost zero. Therefore Q_2 cuts off.

- With Q_2 open, Q_4 goes into cut off and the Q_3 base is pulled HIGH.
- Since Q_3 acts as an emitter follower, the Y o/p is pulled upto a HIGH voltage.
- On the other hand, when A and B both are HIGH the emitter diode of Q_1 are reversed biased making them off.
- This causes the collector diode D_4 to go into forward conduction.
- This forces Q_2 base to go High. In turn Q_4 goes into saturation, producing a low output.

A	A	B	B	Y	Y
0	0	0	0	1	1
0	0	1	1	1	1
1	1	0	0	1	1
1	1	1	1	0	0

- The table summarizes all input & output conditions without diode D_1 in the circuit. Q_3 will conduct slightly when the o/p is low. To prevent this, the diode is inserted, it's voltage drop keeps the base emitter diode of Q_3 reversed biased. In this way, only Q_4 conducts when the o/p is low.

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Active pull up :-

Fig. shows highlighted output configuration Transistor Q_3 and Q_4 form a totem pole. Such a configuration is known as "Active pull up" or "Totem pole output".

- The active pull up formed by Q_3 and Q_4 has specific advantage. Totem pole transistors are used because they produce a low o/p impedance.
- Either Q_3 acts as an emitter follower (High o/p) or Q_4 is saturated (Low o/p).
- When Q_3 is conducting the o/p impedence is approximately 70 Ω, When Q_4 is saturated, the o/p impedence is only 12 Ω. Either way the o/p impedance is low.

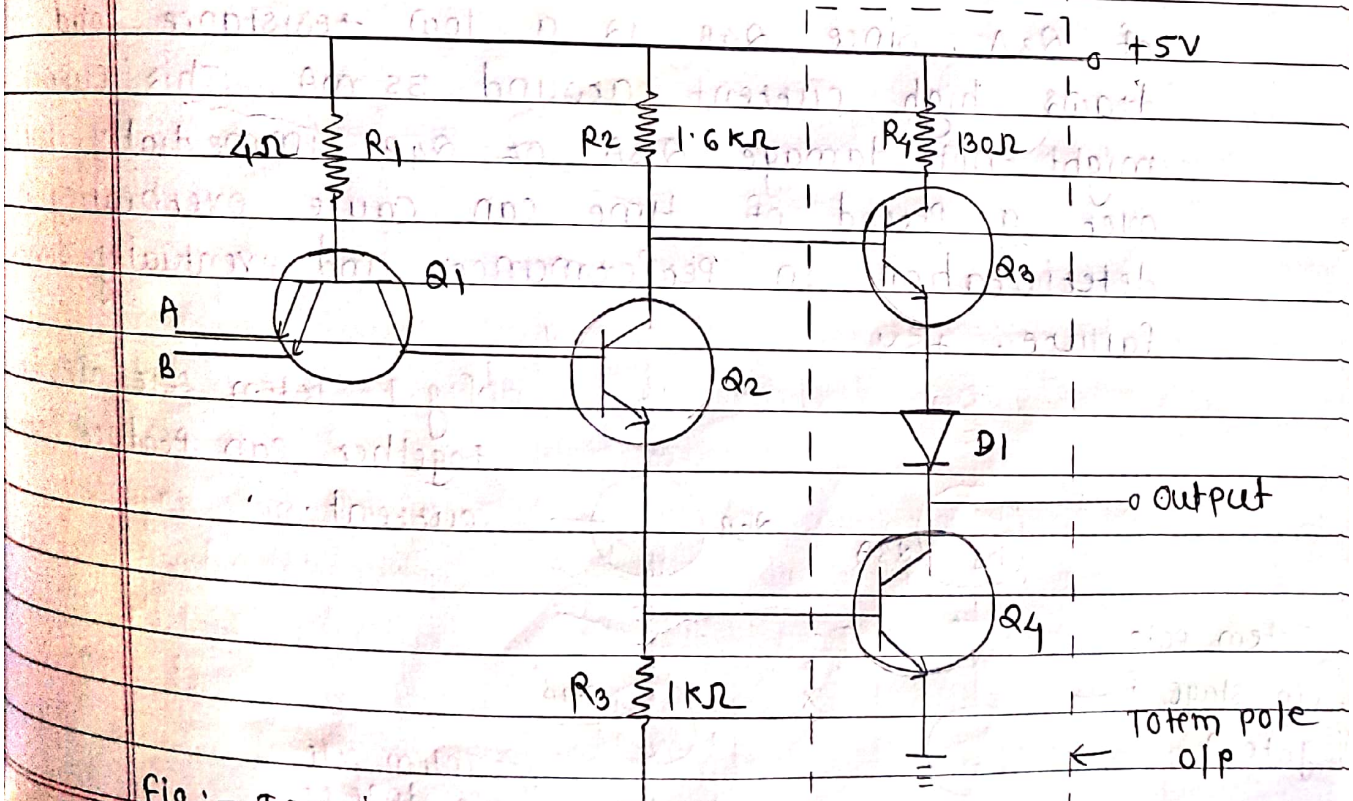


Fig:- Two input NAND gate with totem pole o/p.

This means that the o/p voltage can change quickly from one state to the other because any stray o/p capacitance is rapidly charged or discharge through the low output impedence. Thus the propagation delay is low in totem pole TTL logic.

o Wired logic - Open collector Output :-

- One problem with totem pole output is that two output can not be tied together. Refer fig. 1 where the totem pole outputs of two seperate gates are connected together at point suppose that the output of gate A is high (Q_{3A} ON and Q_{4A} off) and output of B is low (Q_{3B} OFF and Q_{4B} ON).

- In this situation transistor Q_{4B} acts as a load of Q_{3A}. Since Q_{4B} is a low resistance load, it draws high current around 55 mA. This current might not damage Q_{3A} or Q_{4B} immediatly, but over a period of time can cause overheating & deterioration in performance and eventually device failure.

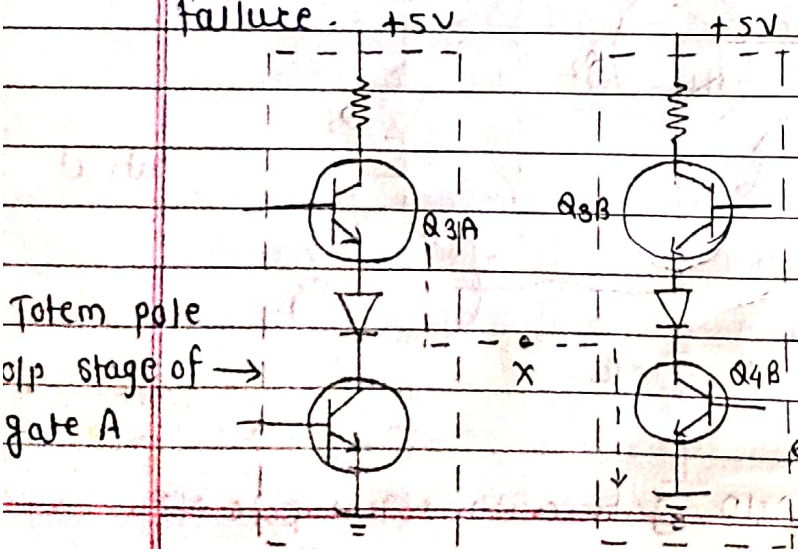
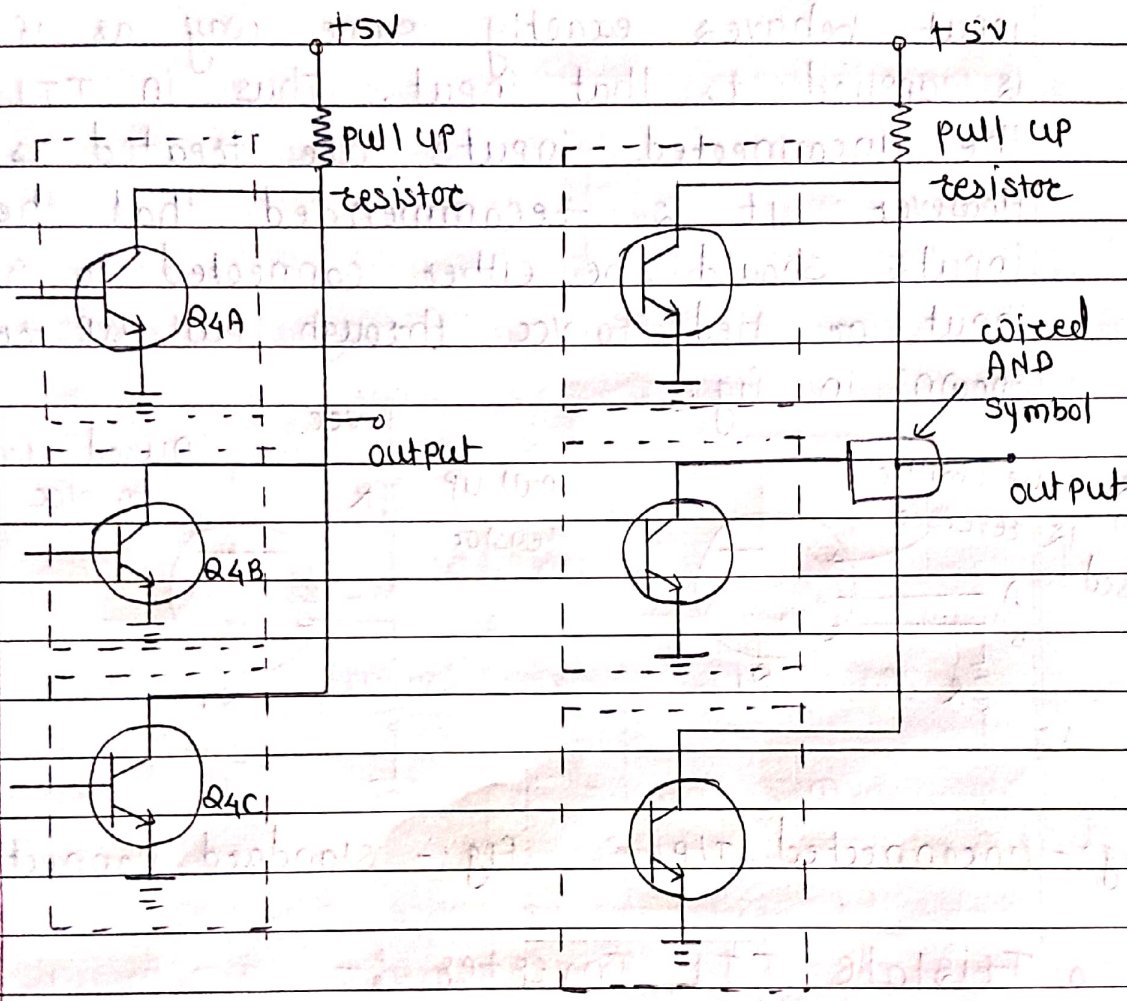


Fig. 1 Totem pole o/ps tied together can produce harmful current.

- Some TTL devices provide another type of output called "open collector output". The o/p's of two different gates with open collector output can be tied together. This is known as "Wired logic"

- This is as shown below :-



(a) open collector outputs connected together (b) Wired AND output with special AND gate symbol.

- The connection is called a wired-AND and represented schematically by the special AND gate symbol as shown in fig. (b).

o Unconnected inputs :-

If any input of TTL gate is left open or unconnected, then the corresponding base emitter junction of the input transistor Q_1 is reversed bias. Therefore the open or unconnected input behaves exactly same way as if a logic 1 is applied to that input. Thus in TTL ICs all the unconnected inputs are treated as logic 1. However, it is recommended that the unused inputs should be either connected to some used input or tied to Vcc through pull up resistor as shown in fig.

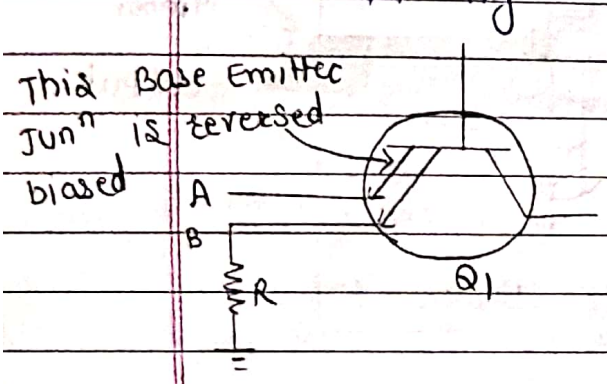


fig:- unconnected I/P

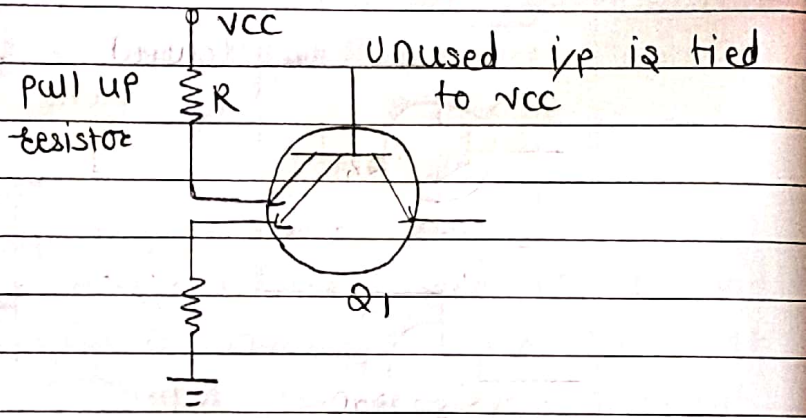


fig:- standard connection.

o Tristate TTL Inverter :-

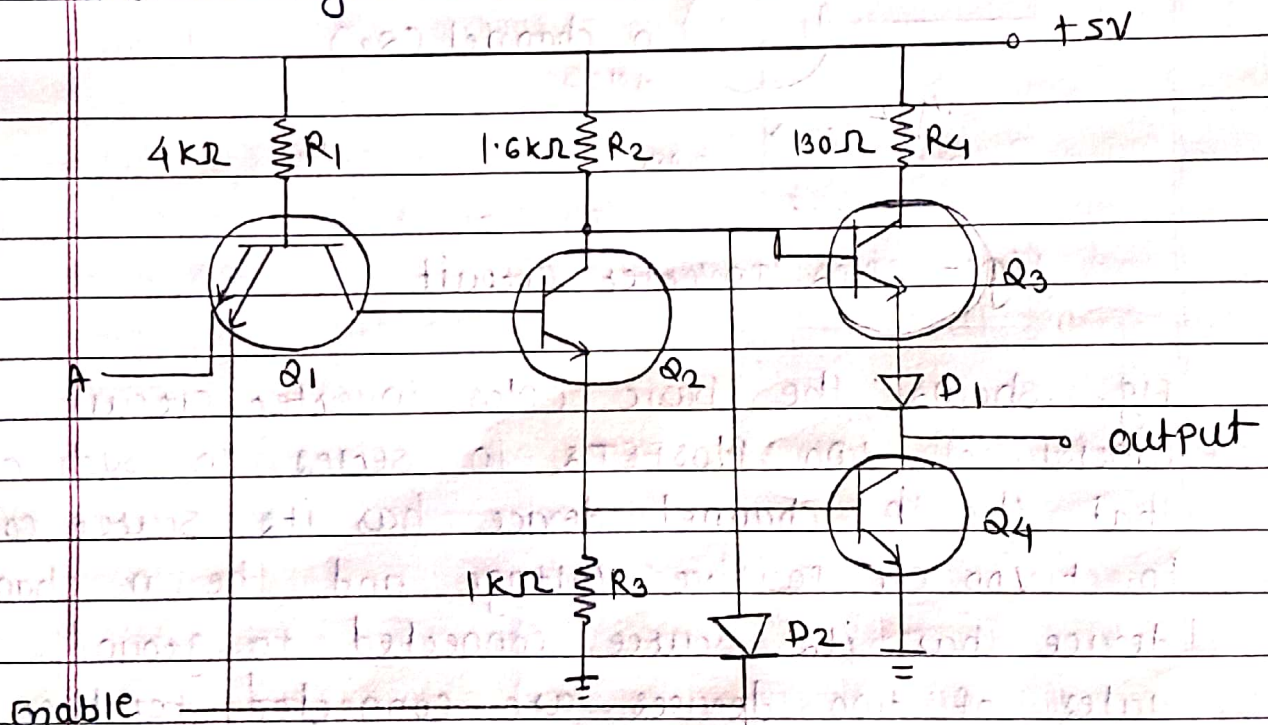
The tristate configuration is a third type of TTL o/p configuration. It utilizes the high speed operation of the totem pole arrangement while permitting outputs to be wired ANDed (connected together). It is called tristate TTL because it allows three possible output stages: High, Low & high impedence.

- We know that transistor Q_3 is ON when o/p is high and Q_4 is ON when o/p is low.

- In high impedence state both transistors Q_3 & Q_4 in the totem pole arrangement are turned off.

- As a result, the o/p is open or floating, it is neither low nor high.

- Fig. shows the simplified circuit for tristate inverter. It has two inputs A and E is the normal logic input & E is an Enable input.



(E) fig:- Tristate TTL inverters.

Truth Table

A	E	output
0	1	1
1	1	0
x	0	floating

CMOS (Complementary MOS) Logic :-

- CMOS circuit contains both NMOS and PMOS devices to speed the switching of capasitive loads. It consumes low power and can be operated at high voltages, resulting in improved noise immunity.

CMOS Inverter :-

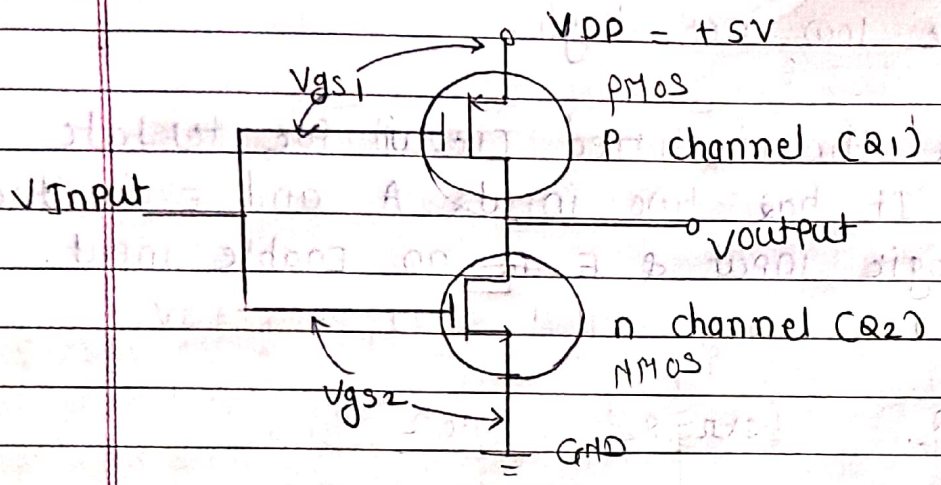


Fig :- CMOS Inverter Circuit

Fig. shows the basic CMOS inverter circuit. It consist of two MOSFETs in series in such a way that the p channel device has its source connected to +VDD (a positive voltage and the n channel device has its source connected to ground. The gates of two devices are connected together as the common ~~devices are connected~~ input and the drains are connected together as the common o/p.

1. When input is high, the gate of Q_1 is at 0V relative to the source of Q_1 i.e $V_{gs1} = 0$. Thus, Q_1 is OFF, on the other hand, the gate of Q_2 is at +VDD

relative to its source $V_{GS_2} = +V_{DD}$. Thus Q_2 is ON. This will produce $V_{out} \approx 0V$ as shown in fig (a)

2. When input is low, the gate of Q_1 is at negative potential, relative to its source while Q_2 has $V_{GS} = 0V$. Thus Q_1 is ON and Q_2 is OFF. This produces o/p v.tg approx. $+V_{DD}$ as shown in fig (b)

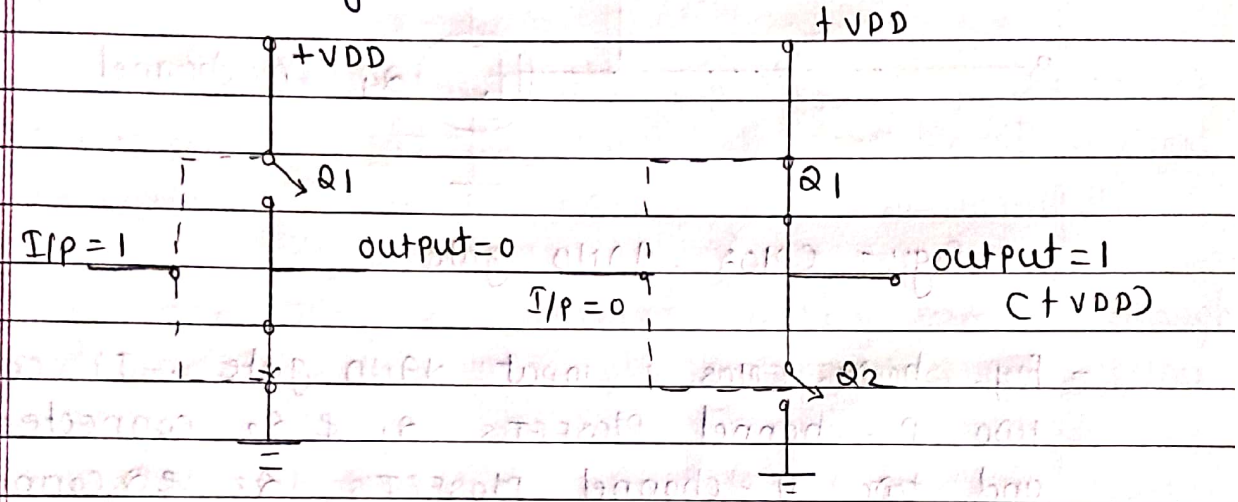


fig (a) Input = 1 fig (b) Input = 0

fig :- Operation of CMOS Inverter for both i/p cond?

The table given below summarized the operation of CMOS Inverter circuit.

A	Q_1	Q_2	o/p
0	ON	off	1
1	off	ON	0

o CMOS NAND gate :-

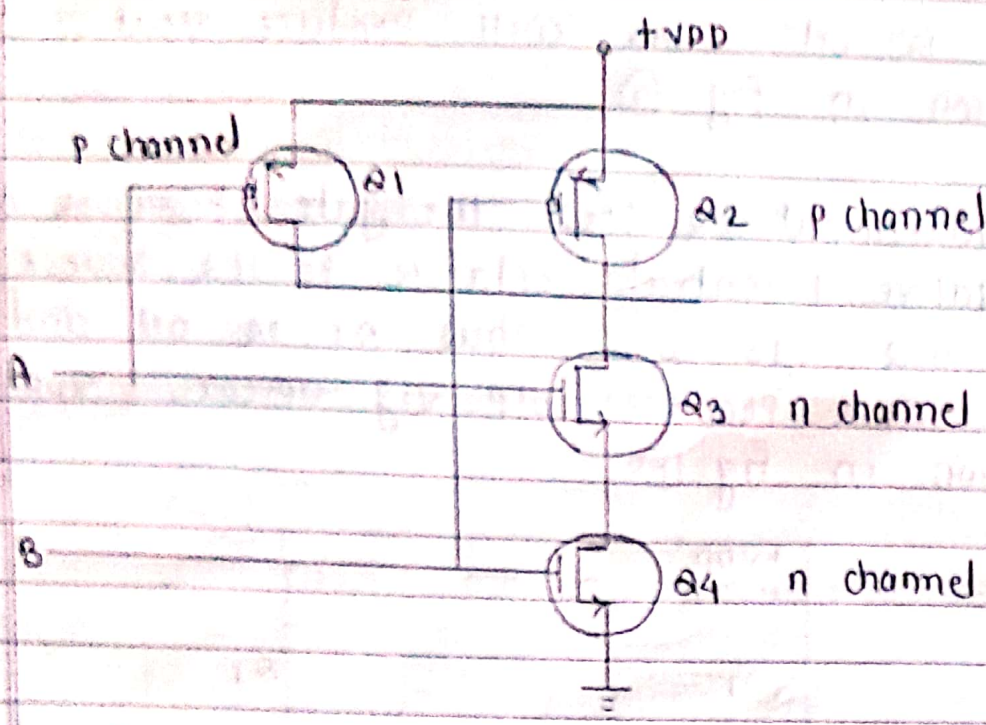


fig:- CMOS NAND gate

- Fig shows CMOS 2 input NAND gate. It consists of two P-channel MOSFETs Q_1 & Q_2 connected parallel and two n-channel MOSFETs, Q_3 & Q_4 connected in series.

- When both inputs are low, the gates of both P-channel MOSFETs are negative with respect to their sources, since the sources are connected to +VDD. Thus Q_1 and Q_2 are both ON since the gate to source voltage of Q_3 and Q_4 (n channel MOSFETs) are both 0V, those MOSFETs are OFF. The o/p is therefore connected to +VDD (High) through Q_1 & Q_2 are disconnected from ground.

- When A = 0 and B = +VDD, Q_2 is ON because $V_{GS1} = -V_{DD}$ and Q_4 is ON because $V_{GS4} = +V_{DD}$

MOSFETs Q_2 and Q_3 are OFF because their gate to source voltages are 0V. Since Q_1 is ON and Q_3 is OFF, the output is connected to $+V_{DD}$ & it is disconnected from ground.

- When $A = +V_{DD}$ and $B = 0V$, The situation is similar, the output is connected to $+V_{DD}$ thr' Q_2 and it is disconnected from ground because Q_4 is OFF.

- Finally when both inputs are high ($A = B = +V_{DD}$), MOSFETs Q_1 and Q_2 are both off and Q_3 and Q_4 are both ON.

- Thus the o/p is connected to the ground through Q_3 and Q_4 and it is disconnected from $+V_{DD}$.

- The table summarizes operation of 2 input CMOS NAND gate.

Table :- Truth table of 2 i/p CMOS NAND gate

A	B	Q_1	Q_2	Q_3	Q_4	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

o CMOS NOR gate :-

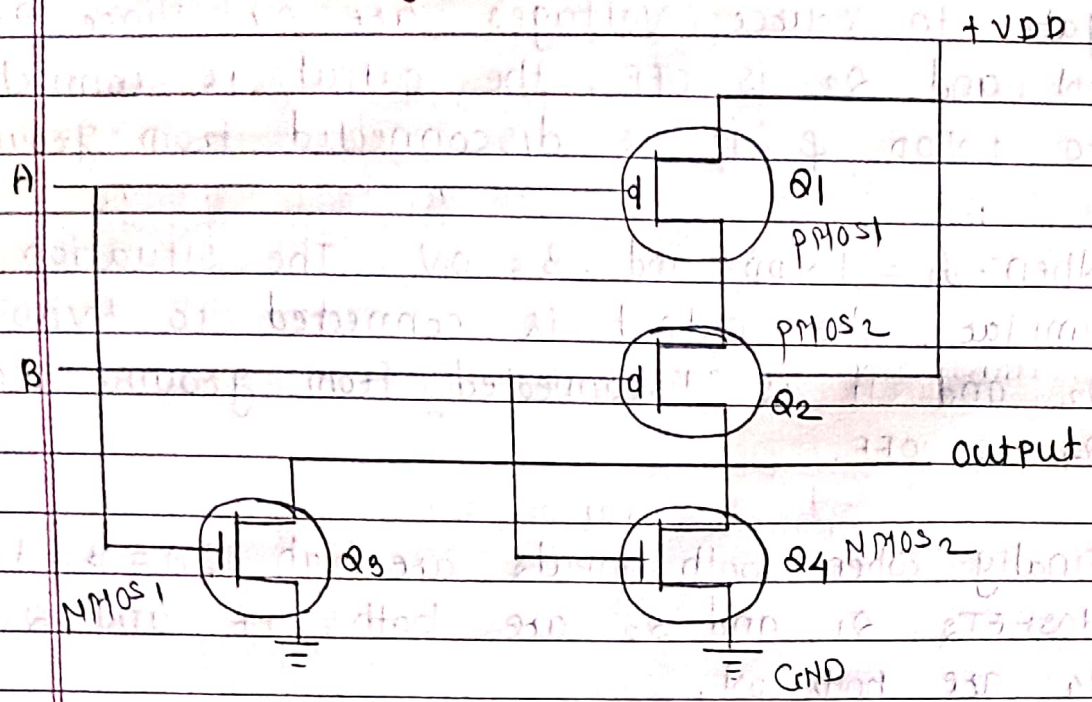


Fig. 2 input CMOS NOR gate.

= Fig. shows 2 input CMOS NOR gate. Here, P-channel MOSFETs Q_1 and Q_2 are connected in series and n channel MOSFETs Q_3 and Q_4 are connected in parallel.

= When the i/p is low, P channel MOSFET turns ON & N-channel MOSFET turns OFF.

- When the i/p is High, P channel MOSFET turns OFF & N channel MOSFET turns ON.

- The operation of 2 input NOR gate can be summarized as given below :-

Table :- Truth table for 2 input NOR gate :-

A	B	Q1	Q2	Q3	Q4	output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

o Unconnected inputs :-

CMOS inputs should never be left disconnects. All CMOS inputs have to be tied either to a fixed voltage level (0V or VDD) or to another input. This rule applies even to the inputs of extra unused logic gates on a chip. An unused CMOS i/p is susceptible to noise and static charges that could ~~MOSFETs in the conductive~~ easily bias both the P - & N - channel MOSFETs in the conductive state, resulting in increased power dissipation and possible over-heating.

o Open drain outputs :-

- CMOS gates are available with open drain outputs. In open drain outputs, PMOS transistor is replaced by a diode D1 which provides protection from electrostatic discharges. open drain gates can be used with external pull up resistors to perform wired AND operation.

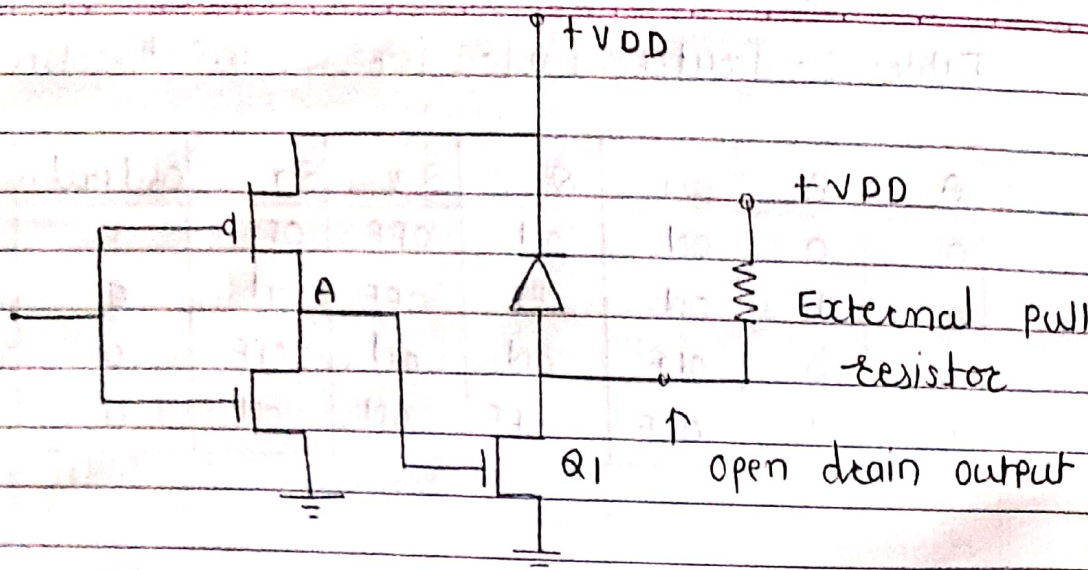


fig :- open drain output

o Interfacing of CMOS and TTL :-

- Interfacing means connecting the o/p(s) of the circuit or system to the input(s) of another circuit or system that may have different electrical characteristics.

- When two circuits have different electrical characteristics direct connection cannot be made. In such cases driver and load circuit are connected through interface circuit. It's fun^n is to take the driver o/p signal and condition it so that it is compatible with requirements of the load.

- One must consider following important points while interfacing two circuits or systems. The driver o/p must satisfy the vtg & clt requirements of the load ckt. The driver & load ckt may require different Power supplies. In such cases the output of both ckt must swing bet^n its specified.

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o Comparison bet^n various logic families / Compari

Sr. No	Parameter	RTL	DCTL	TTL
1)	Component used	Resistor & Transistor	Resistor & Transistor	Resistor, Diode & Transistor
2)	Circuit	Simple	Simplest	Complex
3)	Noise Margin	Poor	Poor	Medium
4)	Fan out	Low (4)	Low (4)	More (10)
5)	Power dissipation in mW per gate	30	30	10
6)	Basic gate	NOR	NOR	NAND
7)	Propagation delay (ns)	12	10	10
8)	Speed power product	144	130	100
9)	Applications	Absolute	Absolute	Laboratory Instruments

Q. Comparison bet^n various logic families / Comparision table of characteristics of TTL, CMOS, ECL, RTL, I^2L, DCTL :-

Sr. No	Parameter	RTL	DCTL	TTL	ECL	I^2L	CMOS
1)	Component used	Resistor & Transistor	Resistor & Transistor	Resistor, Diode & Transistor	Resistor & Transistor	Transistor	N - channel & P - channel MOSFET
2)	Circuit	Simple	Simplest	Complex	Complex	Simple	Moderate
3)	Noise Margin	Poor	Poor	Medium	Low	High	High
4)	Fan out	Low (4)	Low (4)	More (10)	High (25)	8 - 12	50
5)	Power dissipation in mW per gate	30	30	10	40 - 55	5 - 25	0.1
6)	Basic gate	NOR	NOR	NAND	OR - NOR	NAND	NAND / NOR
7)	Propagation Delay (ns)	12	10	10	2 (ECL 10K) 0.75 (ECL 100K)	25 - 250	70
8)	Speed power product	144	130	100	100 (ECL 10K) 40 (ECL 100K)	4	0.7
9)	Applications	Absolute	Absolute	Laboratory Instruments	Due to low propag^n delay they are used in high speed switching application.	Due to high packaging density they are used in LSI functions & large computers	Due to low power consum^n they are used in portable instruments where battery supply is used